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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,581	04/14/2004	Hirotsugu Kojima	XA-10077	6230

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,581	KOJIMA ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *1-4, 12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This a non-Final Office Action in response to the present US Application filed 4/14/2004. Claims 1-13 are pending and presently under examination.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), for JP 2003-182258, filed 06/26/2003. The certified copy has been filed in parent Application No. 10/823,581, filed on 4/14/2004.

Claim Objections

Claims 1-4, 12 and 13 are objected to because of the following informalities

The following Claims are written as hybrid claims, because they include a combination of apparatus and method limitations. Appropriate correction is required.

Claim 1, last paragraph should be amended as follows:

"wherein said nonvolatile memory stores adjustment data for correcting a change in circuit characteristics which occurs due to variations in electronic parts or devices, via said interface circuit for test".

Claim 3, last paragraph should be amended as follows:

"wherein said microcomputer reads the adjustment data stored in said nonvolatile memory".

Claim 12, last paragraph should be amended as follows:

"wherein said nonvolatile memory stores adjustment data for correcting a change in circuit characteristics caused by variations in electronic parts or devices, and data peculiar to the semiconductor integrated circuit, via said interface circuit for test".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, 6, 7, 12, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 6, 7, 12 recite the expression "can be written", which renders the claims indefinite, because it is not clear how a person skilled in the art can write data in the nonvolatile memory, since the claimed invention fails to define ways or means for writing data into the memory.

Claim 3 recites the expression "can be read", which renders the claim indefinite, because it is not clear how a person skilled in the art can read data from the nonvolatile memory, since the claimed invention fails to define ways or means for reading data from the memory.

The claims are generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Applicant should amend the claims accordingly by more clearly pointing out the claimed invention by preferably avoiding using passive voice in defining the various limitations.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Gauthier et al. (US 6,768,955) filed: May 17, 2002.

Regarding independent Claims 1, 12, Gauthier discloses a semiconductor integrated circuit (see Summary of the Invention and Figure 4) comprising:

a rewritable nonvolatile memory, such as a storage device (253) for storing control information representative of the adjustment settings that produce desired operating characteristics of the PLL 280, using the tester 251 to read or rewrite the control information in the storage device 253, which may include multiple storage elements such that the control information may be represented by a binary word that corresponds to values of the k control signals 252. Also, Figure 6a the storage device

253, which includes electrically programmable fuses 604 and 654 to store nonvolatile control information.

An interface circuit for test (test processor unit 250), which controls the adjustment circuits (242 and 244) using k control signals 252. The test processor unit 250 may communicate through a host interface (not shown) using m communication lines 254, which may be defined by an industry standard such as JTAG (IEEE 1149).

Regarding Claim 2, 6, terminals between adjustment circuits 242 and 244 phase locked loop 280 for outputting the adjustment data stored in the storage device 253, which are operatively connected to a charge pump 240 via adjustment control voltages Vcn 246 and Vcp 248, respectively, where the adjustment circuits 242 and 244 are controllable to adjust adjustment control voltages Vcn 246 and Vcp 248 in order to adjust internal biasing voltages within the charge pump 240, thereby adjusting the current output of the charge pump 240.

Regarding Claim 3, 7, Gauthier discloses a microprocessor corresponding to a TAP controller in the test processor unit 250, which is in compliance with industry standard JTAG (IEEE 1149), for communicating through a host interface (not shown) using m communication lines 254. The test processor unit 250, via n signal lines 255, may read the storage device 253 to obtain the control information and determine the amount of adjustment that should occur in adjustment circuit 242 and/or adjustment circuit 244. Accordingly, the PLL 280, after the test processor unit 250 reads the control information in the storage device 253 and adjusts the adjustment circuit 242 and/or

adjustment circuit 244, may have an operating characteristic similar to the operating characteristics obtained while connected to the tester 251.

Regarding Claim 4, 9, 13, Gauthier discloses an electronic part (voltage controlled oscillator 212) comprising a quartz oscillator, which is well known in the art, and using the bias signals Vbp 224 and Vbn 226 to control the voltage controlled oscillator 212, which, in turn, generates the chip clock 204, where the chip clock 204 has a frequency in relation to the bias signal inputs to the voltage controlled oscillator 212. Figure 1 shows a computer system 10, which includes a well known in the art crystal oscillator 18, which generates a system clock signal (also referred to and known in the art as "reference clock"), SYS_CLK, to various parts of the computer system 10.

Regarding independent Claim 5, Gauthier discloses an electronic system, such as a computer system 10, Figure 1, comprising:

an electronic part (crystal oscillator 18, Figure 1, and also shown in Figure 4 as the voltage controlled oscillator 212), and a first semiconductor integrated circuit (16, Figure 1 and also described in the Summary of the Invention in reference to Figure 4 as the integrated circuit), including:

a rewritable nonvolatile memory, such as a storage device (253) for storing control information representative of the adjustment settings that produce desired operating characteristics of the PLL 280, using the tester 251 to read or rewrite the control information in the storage device 253, which may include multiple storage elements such that the control information may be represented by a binary word that corresponds to values of the k control signals 252. Also, Figure 6a the storage device

253, which includes electrically programmable fuses 604 and 654 to store nonvolatile control information.

An interface circuit for test (test processor unit 250), which controls the adjustment circuits (242 and 244) using k control signals 252. The test processor unit 250 may communicate through a host interface (not shown) using m communication lines 254, which may be defined by an industry standard such as JTAG (IEEE 1149).

Regarding Claim 8, a read only memory (ROM) by describing "that the storage device 253 may contain a wide variety of types of storage elements including, but not limited to, an electrically programmed fuse, an electrically programmed read only memory (EPROM), an electrically erasable read only memory, a one time programmable memory, a flash memory, a laser programmed fuse, and a laser programmed anti-fuse.

Regarding Claim 10, Gauthier discloses phase locked loop (PLL) 200, which receives system clock SYS_CLK 202, and generates a reference clock signal (chip clock signal, CHIP_CLK), 204, Figures 1, 3a and 4. Also, as shown in Figure 1, PLL 20 is used within the computer system 10 to ensure a proper reference of time among a system clock, by controlling an oscillator such that the oscillator maintains a constant phase relative to a reference signal, which receives a SYS_CLK, from crystal oscillator 18 and outputs a chip clock signal, CHIP_CLK, to the microprocessor 12.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gauthier et al. (US 6,768,955) in view of Lin (US 6,975,840).

Regarding Claim 11, Gauthier does not explicitly disclose, "a semiconductor integrated circuit for RF having a transmission/reception function".

In analogous art, Lin (US 6,975,840) discloses a Radio Frequency (RF) interface 154 for RF communications of wireless device 150, which includes an RF transmitter 156 and an RF receiver 158, both couple to an antenna 160 and to a baseband processor 164, Figures 1B and 2. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to deploy a Radio Frequency (RF) interface as taught by Lin, in the computer system of Gauthier for use with RF wireless communication systems including such as cellular systems and wireless local area networks, which typically built to support operating standards. Thus, by complying with these operating standards, equipment interoperability is achieved.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: 4/6/06

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Office Action: Non-Final Rejection